REMARKS

Present Status of Application

The Examiner is thanked for his continued indication that claims 3-7, 10-14, and 17-20 are allowable. The Office Action, however, rejected claims 1, 2, 8, 9, 15, and 16 under 35 U.S.C. § 103(a) as allegedly unpatentable over U.S. Patent 5,936,868 to Hall. For the reasons set forth below, Applicant respectfully requests that the rejection be withdrawn.

Summary of Present Application

The present application is directed to a method and apparatus for evaluating a gate of an integrated circuit to determine whether or not the gate has acceptable immunity to noise. The apparatus comprises a computer configured to execute a rules checker program, which receives input relating to characteristics of a static gate contained in the integrated circuit. The gate comprises at least two field-effect transistors (FETs). Each FET has a width and the characteristics received in the input to the rules checker program include the widths of the field effect transistors. The rules checker program analyzes the widths of the FETs to determine whether or not the gate has an acceptable level of noise immunity.

Each gate typically comprises a plurality of FETs, usually an NFET and a PFET, and input terminals for receiving input signals. The rules checker program processes the widths of the PFETs and NFETs to obtain at least a first numerical value relating to the widths. The rules checker program utilizes the first numerical value to access one or more threshold noise-level values from a memory device in communication with the computer. The rules checker program determines noise levels on the inputs, either through calculation or simulation. The rules checker program compares the determined noise levels with the threshold values and

uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

Discussion of Office Action Rejections

Applicant respectfully traverses the rejections and submits that they should be withdrawn.

Discussion of Rejection of Claims 1, 2, 15, and 16

The Office Action rejected independent claims 1 and 15 under 35 U.S.C. § 103(a), as allegedly unpatentable over U.S. Patent 5,936,868 to Hall. Applicant respectfully traverses this rejection for at least the reasons that follow.

Turning first to independent claim 1, independent claim 1 recites:

> 1. An apparatus ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the apparatus comprising:
> a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, ***the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity***.

Likewise, claim 15 recites:

> 15. A computer-readable medium containing a rules checker computer program, the computer program ***evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:
> ***code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully traverses the rejection of independent claims 1 and 15 for at least the reason that the cited art fails to disclose or teach at least the features emphasized above.

The Office Action alleged that Hall teaches these features (or an obvious variant thereof). Applicant respectfully disagrees. In this regard, Hall is directed to a system and method for converting an integrated circuit design for an upgraded process. Specifically, Hall is directed to a system and method that automates the re-design of an integrated circuit for an updated manufacturing process. In the process of Hall, multiple downward size scalings are first performed (to downward scale contacts and vias) before performing an upward size scaling.

Relevant to claimed features of the present application, however, the system and method of Hall does not teach an analysis or determination of noise immunity, as claimed by the presently pending claims. In fact, the only reference to, or acknowledgement of, noise in the Hall patent is in the context of a "noise ratio." Specifically, this noise ratio refers to a noise ratio between the original manufacturing process and the updated manufacturing process. If the original circuit design was subject to a certain level of noise, this level may differ in the update process, based on the change in dimensional scales between the original design and the updated design. This difference is referred to in Hall as a noise ratio. (See, e.g., col. 4, lines 46-57).

Returning to specific features defined in independent claims 1 and 15, claim 1 specifically defines "***the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.***" Likewise, claim 15 specifically defines ***"code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity."*** These

elements are neither taught nor suggested by Hall. It appears that the Office Action has confused certain teachings of the Hall patent, in applying this reference to reject claims 1 and 15 of the present application. To illustrate, Applicant notes with emphasis the teaching with Hall at col. 4, lines 37-56, which states:

> Yet another important aspect of the invention relates to the treatment of the supply rails. In other words, the method may further comprise the step of selectively performing a fifth upward ***size scaling on the mask data in at least one dimension to scale up at least one of the power supply rails***. The step of selectively performing the fifth upward scaling preferably comprises displaying and viewing an image of the IC design, and selecting the power supply rails based on displaying and viewing the image. Moreover, the step of the fourth upward size scaling for the power supply rails preferably comprises the step of determining a scaling factor based on a desired voltage noise ratio between the original process and the updated process.
>
> ***In another embodiment relating to the treatment of the supply rails, the method includes determining a desired width upward scaling factor based on a desired voltage noise ratio between the original process and the updated process, and selectively adding at least one additional parallel supply rail based upon determining that the desired width upward scaling factor is greater than about two.***

(*Emphasis added.*) Thus, while this portion of Hall mentions the terms "width" and "noise," it is not referring to the FET width or noise immunity, as claimed in claims 1 and 15. Instead, the "width" that Hall is referring to is a dimensional width for applying an upscaling factor (while holding a length of a second dimension constant during the upscaling). Likewise, the noise that Hall is referring to us a noise ratio between the power supply rails of an original process and an updated process (where the update process results from the collective downscaling and upscaling steps of the method of Hall).

The Office Action also referenced column 7 line 21 through column 8, line 25 in support of its application of Hall to the claims. There, the description in Hall makes reference to the channel length of a MOS device. Specifically, Hall states that "additional intervention" may be required to ensure that the scaling does not reduce a channel length to a smaller (or shorter) size that that which is allowed by the fabrication process (col. 7, lines 21-24). Stated

another way, Hall recognizes that, if the mathematical portion of the scaling process would generate a circuit design requiring smaller dimensions than the fabrication process would support, then additional intervention would be required. This, however, is unrelated to the claimed features of claims 1 and 15, which have been emphasized.

The Office Action further references the teaching of col. 8, lines 12-26 as allegedly teaching "the design rule checker program is to check transistor noises such as transient noise, noise levels, etc." Applicant respectfully disagrees. This portion of Hall specifically states:

> A plot of Vss (ground) metal ratio (w_x / w_n) for a CMOSN part converted to a CMOSX (0.8 μM) part is shown in FIG. 6 for Vdd_n =5.0 V and ξ=1. Similarly, FIG. 7 shows the requirements for Vdd distribution. Note that the conversion of a CMOSN part in a 5V application to a CMOSX (0.8 mm) part in a 3.3V application requires no change to either the ***Vdd (power) or the Vss (ground) distribution width if the allowable noise levels on the distributions in the two cases are identical.*** If the maximum operating voltage of the converted IC is limited to 3.3V, no power or ground metalization adjustment needs to be made in the conversion process; however, if operation at 5V is required to be maintained, then an adjustment is required as shown in the cell 25A, 25B and 25C of FIGS. 5A, 5B and 5C, respectively.

(*Emphasis added.*)

This portion of Hall (along with the equations at the bottom of col. 7) teaches an assessment of MOS channel width/length ratios in comparison to the ratio of original process to the updated process to determine whether a distribution width of either Vdd (power) or Vss (ground) needs to be changed. That is, Hall does not teach or disclose the determination of whether a gate is susceptible to noise immunity by evaluating the widths of the field effect transistors that comprise the gate. Instead, Hall teaches only the evaluation of circuit and device parameters to determine whether a noise ratio (resulting from a circuit scaling conversion) is within acceptable limits, or whether a dimensional limitation in the scaling process will need to be changed.

Simply stated, Hall does not teach or disclose ***analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity***. Consequently, the rejections to independent claims 1 and 15 should be withdrawn.

Since rejected claims 2 and 16 depend from independent claims 1 and 15, the rejections to these claims should be withdrawn for at least the same reason.

Discussion of Rejection of Claims 8 and 9

The Office Action also rejected claims 8 and 9 under 35 U.S.C. § 102(e), as allegedly obvious over Hall. Applicant respectfully traverses this rejection for at least the reasons that follow.

Independent claim 8 recites:

> 8. A method ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the method comprising the steps of:
>
> receiving input in a computer relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors; and
>
> ***analyzing the widths of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity***.

(*Emphasis added.*) Applicant respectfully traverses the rejection of claim 8 for at least the reason that Hall fails to disclose or teach either of the features emphasized above.

The Office Action rejected claim 8, relying on the same portions of Hall that the Office Action relied upon in rejecting claim 1. In this regard, the Office Action relied principally upon the teachings in columns 7 and 8 of the Hall patent. Simply stated, and for the same reasons discussed in connection with claims 1 and 15 above, Hall does NOT teach at

least the features of claim 8 that are emphasized above (i.e., "evaluating a gate to determine whether or not the gate has an acceptable immunity to noise" or "analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity."

Consequently, and for the same reasons set forth in connection with claim 1, Applicant respectfully submits that the rejection of claims 8 is misplaced and should be withdrawn. For at least these same reasons, claim 9, which depends from claim 8, patently defines over Hall as well.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to Hewlett-Packard Company's deposit account No. 08-2025.

Respectfully submitted,

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Please continue to send all future correspondence to:

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